CLAIMS

What is claimed is:

1. A receiving apparatus comprising:

one or more variable gain amplifiers;

one or more level detection circuits, at least one which detects one or more levels output from at least one of the variable gain amplifier or amplifiers;

one or more comparing circuits comparing to one or more reference levels one or more outputs from at least one of the level detection circuit or circuits;

one or more demodulators;

one or more binarizing circuits;

one or more gain switching detection circuits detecting switching of one or more gains of at least one of the variable gain amplifier or amplifiers;

one or more slice level holding circuits holding at one or more substantially constant values one or more slice levels employed by at least one of the binarizing circuit or circuits; and

one or more counter circuits;

wherein at least one gain of at least one of the variable gain amplifier or amplifiers is switched based on at least one result of comparison by at least one of the comparing circuit or circuits; and

wherein, when switching of at least one of the gain or gains is detected by at least one of the gain switching detection circuit or circuits, at least one of the counter circuit or circuits and at least one of the slice level holding circuit or circuits cause at least one of the slice level or levels to be held at at least one of the substantially constant value or values for one or more prescribed times.

2. A receiving apparatus according to claim 1 in which at least one of the variable gain amplifier or amplifiers also serves as at least one bandpass filter.

3. A receiving apparatus according to claim 1 in which at least one of the comparing circuit or circuits also serves as at least one gain switching detection circuit.

4. A receiving apparatus according to claim 1 in which at least one time counted by at least one of the counter circuit or circuits is variable.

5. A receiving apparatus according to claim 1 in which at least one of the binarizing circuit or circuits comprises:

one or more minimum value detection circuits and one or more maximum value detection circuits accepting input of one or more demodulated signals from at least one of the demodulator or demodulators by way of one or more demodulated signal holding circuits and respectively detecting one or more minimum values and one or more maximum values of at least one of the demodulated signal or signals input thereto;

one or more adding circuits adding at least one of the minimum value or values and at least one of the maximum value or values;

one or more amplifiers substantially halving at least one output of at least one of the adding circuit or circuits; and

one or more comparing circuits carrying out binarization by comparing at least one magnitude of at least one output from at least one of the amplifier or amplifiers and at least one magnitude of at least one of the demodulated signal or signals from at least one of the demodulator or demodulators;

at least one of the demodulated signal holding circuit or circuits functioning as at least one of the slice level holding circuit or circuits.

6. A receiving apparatus according to claim 1 in which at least one of the binarizing circuit or circuits comprises:

one or more offset canceler circuits outputting, when one or more signals input thereto is or are less than one or more lower cutoff values, at least one signal corresponding to at least one amount by which at least one of the signal or signals input thereto is less than at least one of the lower cutoff value or values, and/or outputting, when one or more signals input thereto is or are greater than one or more upper cutoff values, at least one signal corresponding to at least one amount by which at least one of the signal or signals input thereto is greater than at least one of the upper cutoff value or values;

one or more integrating circuits integrating at least one of the output or outputs therefrom;

one or more offset canceler output holding circuits provided between at least one of the offset canceler circuit or circuits and at least one of the integrating circuit or circuits;

one or more adding circuits adding and feeding back one or more outputs from at least

one of the integrating circuit or circuits to one or more input signals; and

one or more sign determining circuits using the sign of at least one signal output from at least one of the adding circuit or circuits to carry out binarization;

at least one of the offset canceler output holding circuit or circuits functioning as at least one of the slice level holding circuit or circuits.